ABSTRACT OF THE DISCLOSURE

In accordance with an embodiment of the present invention, a triggering event is initiated to place a processor in a low power state. The processor may or may not flush a cache upon entering the low power state depending on a power status signal. The power status signal may indicate the relative priority of power reduction associated with placing the processor in the low power state without first flushing the cache versus an increase in soft error rate in the cache associated with reducing the voltage in the low power state.